REMARKS

Claims 50-97 were pending in the above-referenced application. Such claims stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1, 3, 6, 23-24 and 26 of U.S. 6,157,396 to Margulis et al. Claims 50-72, 74-93 and 95-97 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. 6,157,396 to Margulis et al., and Claims 73 and 94 stand rejected under 35 U.S.C. §103(a) as being unpatenable over U.S. 6,157,396 to Margulis et al.

With regard to the double patenting rejection, Applicant provides a Terminal Disclaimer and a copy of the Assignment of the instant application to Pixonics, LLC, filed concurrently herewith. Upon recordation of the Assignment, the instant application and U.S. 6,157,396 will be commonly owned and such Terminal Disclaimer will be effective to overcome the double patenting rejection.

With regard to the rejections under §§102 and 103, Applicant directs the Examiner to section entitled "Cross-Reference to Related Applications" on page 1 of the instant application and to the originally filed Declaration. Both the application and the Declaration clearly claim priority for the instant application to U.S. Provisional Application No. 60/096,322 which was filed on August 12, 1998. As such priority application predates the filing date of the cited U.S. 6,157,396, such cited patent is not a proper reference for the Examiner's statutory

rejections. It necessarily follows then that such rejections must be withdrawn, which action is earnestly sought.

A copy of Provisional Patent Application No. 60/096,322 is provided herewith for the Examiner's reference. Referring to pending Claim 50, which recites:

> An image processing apparatus for receiving bitstream data and processing said bitstream data to provide video stream image data to a display device, comprising:
>
> a display input processor (DIP) coupled to a databus, said DIP comprising an input data connector and a first plurality of processing modules configured to receive bitstream data input and reconstruct said input to generate DIP outputs;
>
> a display output processor (DOP) coupled to said databus, said DOP comprising a second plurality of processing modules configured to process said DIP outputs for generating DOP outputs, said second plurality comprising a geometric transformation (GT) module and a post GT filtering module; and
>
> a buffer memory, coupled to said databus, configured to store said DIP outputs and said DOP outputs, and to provide said video stream image data to said display device.

Applicant directs the Examiner to Fig. 2 of the Provisional Application which depicts display input processor or DIP 210 coupled to bus 212 for receiving data and coupled to bus 214 for sending data to display output processor or DOP 230. Description of this figure is on page 10 of the Provisional Application. Referring now to Fig. 3, a more detailed representation of DIP 210 is provided depicting that DIP 210 comprises a plurality of processing modules, including Analog Data module 300, Digital Data module 304, Compressed Data module 312, Image Reconstruction module 308 and Decompression module 314. It is

further noted that such figure corresponds to Fig 3 of instant application where Digital Data 302 is renumbered as Digital Input Control 304 and the internal bus 304 is renumbered as Databus 350. At pages 10-13, these modules are further described in a manner comparable to that at page 16, line 4 through page 18, line 12 of the instant application. Thus Figs. 2 and 3 of the instant application and the recited aspects of the DIP in Claim 50, are fully supported in the Provisional Application.

Turning now to Fig. 4 of the Provisional Application, a detailed view of the digital output processor or DOP 230 is shown. It is seen that DOP 230 comprises another plurality of processing modules which specifically include a geometric transform module 404 and a post GT filtering module 410. The Examiner is also directed to the Provisional Application at pages 13-15 where Fig. 4 is specifically described. Applicant again notes that such figure and description are comparable to that of Fig. 4 in the instant application as well as the description of that figure beginning on page 26, line 15. Therefore the recited aspects of the DOP in Claim 50 are also fully supported in the Provisional Application.

Finally Claim 50 recites a buffer memory coupled to both the DIP and the DOP. Such Buffer Memory 220 is shown in Fig. 2 of the Provisional Application having double headed arrows to indicate the coupling to each of the DIP 210 and DOP 230. Hence this final aspect recited in Claim 50 of the instant application also finds support in the

Provisional application. In a similar manner, the other claims of the instant application find support in the referred to Provisional Application, hence it is indisputable that the instant application is entitled to the priority of such Provisional Application.

In summary, Applicant has filed herewith a properly executed Terminal Disclaimer to overcome the double-patenting rejection. In addition, Applicant has noticed the Examiner of the filing date of the priority application to the instant application which has a filing date before that of the patent cited as prior art. Applicant has further shown that the instant application is a derivative of the Provisional Application and is thus entitled to the priority date it affords. Therefore, Applicant respectfully asserts that Claims 50-97 are all in condition for immediate allowance, which action is earnestly requested. If the Examiner's next action is to be anything other than a Notice of Allowance, the undersigned respectfully requests the Examiner call the undersigned to schedule a telephonic interview prior to the mailing of such an action.

Respectfully submitted,

Dated: May 15, 2001 By: _____
Bernard Berman
Reg. No. 37,279